Single-Chip 20-GHz VCO and Frequency Divider in SiGe Technology

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Abstract— **This paper presents the design, implementation and testing of a fully integrated 20 GHz voltage controlled oscillator, a frequency divider with a divide ratio of 16, as well as an output driver. All blocks are integrated on one IC with an area of 890 x 890 μm^2 and are fabricated in a production SiGe bipolar technology. The VCO is a varactor-tuned LC-type oscillator with a tuning range of 600 MHz. The differential signal of the output driver is converted to a single-ended signal by an external microstrip balun and delivers a maximum of 2 dBm of output power into a 50 Ω load. The chip works with a single supply voltage of 3.6 V, the VCO draws 12 mA of supply current, divider and output driver consume 17 mA and 51 mA, respectively. The measured phase-noise of the VCO is -85 dBc/Hz at 1 MHz offset frequency.**

I. Introduction

While traditionally frequency generation components employed in RADAR distance-sensors relied on the use of expensive III-V semiconductor technology, like Gunn-oscillators ([4]), in the past years due to advancing reduction of feature size and sophisticated process technologies, Si and especially SiGe has evolved to bridge the gap. Several circuits operating around and above 20 GHz have been demonstrated ([1]-[3]). In the following, to the authors knowledge for the first time, a fully integrated combination of a voltage controlled oscillator and a frequency divider with a division ratio of 16 as well as an output driver in a production SiGe technology (Infineon Technologies B7HF) operating at 20 GHz is reported. The chip is intended to be used in a RADAR transmitter (e.g. FMCW), where it will be combined with a phase-locked loop (PLL) for ease of generation of linear sweeps. Integration of the frequency divider together with the VCO on one chip enables the utilization of a standard PLL-chip with an operating frequency of about 1.5 GHz. In case the VCO is used outside of a PLL as a free-running oscillator, measuring the output frequency is strongly simplified by the frequency divider. Due to the on-chip output driver it is possible to directly drive loads such as an antenna in a short distance industrial RADAR-sensor without the need for an external amplifier.

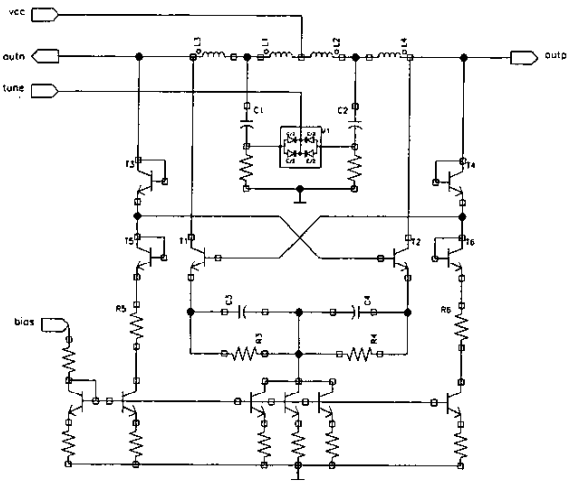

Fig. 1. Simplified schematic of the differential, varactor-tuned LC-type VCO.

II. Circuit Design

A. Voltage Controlled Oscillator

A simplified schematic of the LC-type oscillator is shown in Fig. 1. The core of the VCO consists of a negative resistance generator, formed by a cross-coupled differential amplifier (T_1, T_2). Diode connected transistors T_3 and T_4 in the feedback path, essentially emitter followers with shorted base-collector diodes, reduce the loading of the resonant tank and increase the collector-emitter voltage of T_1 and T_2, thereby augmenting their transit-frequency. To prevent upconversion of flicker-noise generated by T_1 and T_2 by the nonlinearity of the differential amplifier, the diff-pair is degenerated with emitter-resistors R_3 and R_4, to linearize the ampflifier for low frequencies. For high frequencies the emitter degeneration is bypassed by capacitors C_3 and C_4 to achieve high negative resistance at the oscillation frequency. Fig. 2(a) depicts the resonant tank of the VCO, which consists of an inductor, 2

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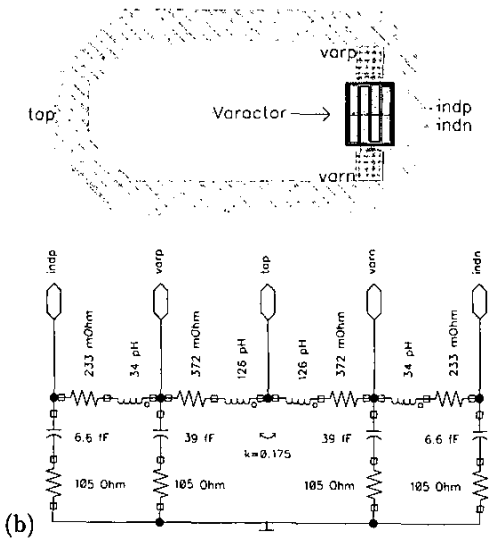


Fig. 2. (a) Layout of the integrated tank with inductor and varactor. (b) Equivalent circuit of the inductor with connections for the varactor.

metal-insulator-metal (MIM) capacitors (C_1, C_2) and varactor V_1 for frequency tuning. The inductor consists of a 20 μm wide U-shaped line in the thick top-metal layer. The wide line minimizes series-resistance at the cost of slightly decreased inductance per length and added parasitic capacitance to the substrate. A compact layout of the tank is achieved by putting the varactor as well as the MIM capacitors into the inside of the inductor. Also shown in Fig. 2(b) is the equivalent circuit of the inductor. Inductance and resistance were computed with the field-solver Fasthenry ([5]), parasitic oxide-capacitances and substrate-resistances were estimated from the geometry of the inductor. The structure of the tank demands the introduction of two additional terminals (varp, varn) to the equivalent circuit, to account for the connection to the MIM-capacitors and varactor. Simulations of the overall quality factor of the tank resulted in a Q of about 5.

B. Output Driver

The circuit schematic of the output driver implemented on the chip is shown in Fig. 3. Due to the inverse proportionality of the current gain β to the operating frequency f ($\beta \approx \frac{f_t}{f}$), maximum possible current gain at 20 GHz is approximately 3 with a given maximum transit-frequency of 75 GHz of the SiGe technology used. To obtain a high output current swing and simultaneously maintain a high input impedance of the driver circuit, several transistor stages have to be cascaded, increasing the bias current with each

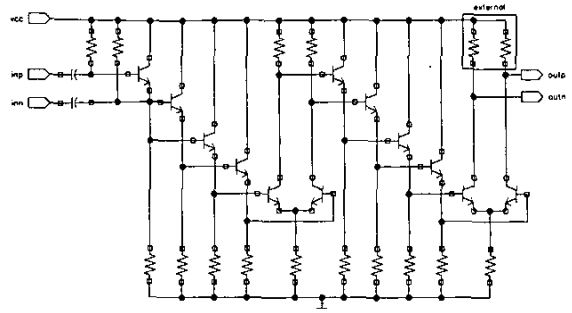


Fig. 3. Circuit schematic of the output driver.

stage. Therefore, the present output-driver consists of two pairs of emitter-followers driving a differential amplifier, another two pairs of emitter followers and finally a differential amplifier with open collector outputs, which is biased at 32 mA total current. The collector resistances shown in Fig. 3 represent external 50 Ω terminations. It should be mentioned that no on-chip output terminations are provided, which might be necessary to reduce double reflections at the output in the presence of mismatched loads. A version with 50 Ω output resistors can, however, be readily fabricated by means of focussed ion-beam implantation of two short metal lines, since 50 Ω resistors are provided on the chip. All transistors used in the driver and in the frequency divider are carefully selected according to their optimum collector-current density for maximum transit-frequency ($j_{C,opt}$) in order to optimize performance, minimize current consumption and the total number of stages in case of the output driver.

C. Frequency Divider

The frequency divider consists of an input buffer (2 pairs of emitter-followers), four cascaded master-

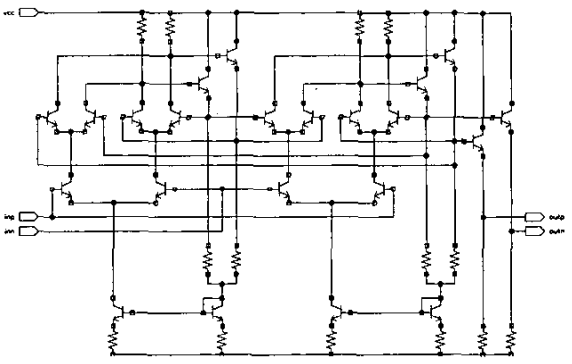


Fig. 4. Circuit schematic of a master-slave T-flip-flop used in the frequency divider.

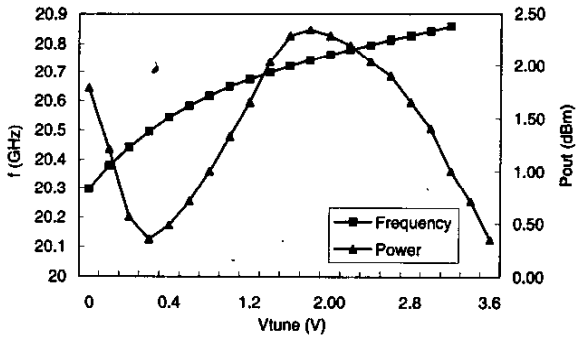
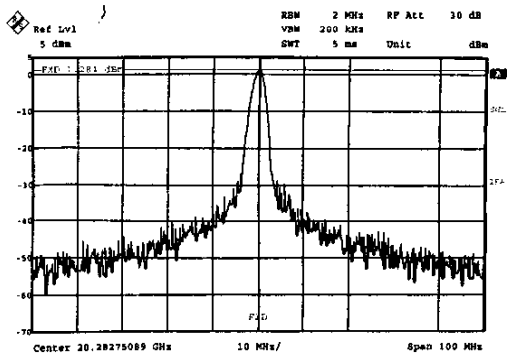


Fig. 5. Oscillation frequency and output power as a function of varactor tuning voltage.

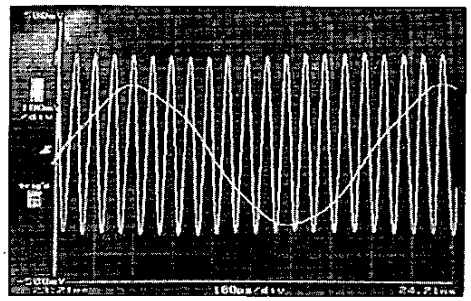
slave T-flip-flops (TFFs) and a differential amplifier as output stage. Fig. 4 shows a schematic of a TFF in emitter-coupled-logic (ECL) used in the frequency-divider. Emitter followers are used after master and and slave, respectively, in order to reduce the loading of the collector-nodes of the latches and increase the collector-emitter voltages of the transistors. The layout of the divider was optimized towards minimum and symmetric parasitic capacitances, especially of all lines connecting from and to the collector nodes of the upper differential pairs. As a measure to minimize total current consumption, all four divider stages operate with a differential voltage swing of 2 x 200 mV_{pp}. Apart from different bias-resistors and load-resistors of the latches, all four TFFs have identical transistor size and layout. Total current consumption of the divider is 17 mA, of which 8 mA are consumed by the first TFF operating at 20 GHz. The current consumption can be further reduced by omitting the emitter-followers of the lower frequency stages.

III. Implementation and Measurements

The circuit was fabricated in Infineon Technolgies B7HF process, featuring high-frequency transistors with cut-off frequencies up to 75 GHz, integrated varactors and MIM-capacitors and thick top layer metallization. Fig. 7 shows a microphotograph of the chip. The die size is 890 x 890 μm^2, the signal pads of the VCO are relatively large to facilitate on-wafer measurements. Presenting a capacitive load of about 70 fF (corresponding to an impedance of 113 Ω at 20 GHz), they lower the available output power significantly. This effect can easily be reduced by using minimum-sized bond-pads, if on-wafer probing is not desired. For testing purposes the chip was mounted on a brass block, surrounded by blocking capacitors and 0 Ω resistors for connection of the ground-pads to the brass block,



(a)



(b)

Fig. 6. (a) Measured spectrum of the VCO at a tuning voltage of 0 V. Phasenoise is approximately -85 dBc/Hz at 1 MHz offset. (b) Measured transient output voltages of VCO and frequency divider.

which also acts as the ground plane for the microstrip circuits of the external circuitry. Differential to single ended conversion of the VCO outputs is achieved by an external microstrip ratrace balun with a center frequency of 20 GHz, fabricated from RT/Duroid. A separate test-structure with two baluns mounted in a back-to-back configuration was used to test the balun. Measurements proved the transmission loss in this configuration to be better than 2.5 dB over a wide frequency range from 14 to 23 GHz. A K-connector at the output connects the chip to the external bias-T needed to bias the open collector outputs of the driver. The balun is shown in the upper part of Fig. 8. In the lower part, the output of the frequency divider as well as SMA-connectors for the tuning voltage and the supply voltages can be seen. The chip is mounted in the center of the brass-block and wire-bonded to gold-plated high-frequency microstrip and DC supply-lines. When no input signal is applied to the frequency divider (i.e. no supply voltage for the VCO), the frequency divider resonates at its self-resonance frequency due the feedback of the output of each TFF to its own input. The measured self-resonance frequency of the

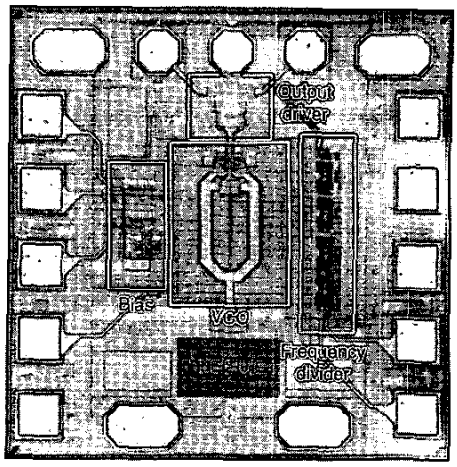


Fig. 7. Microphotograph of the fabricated chip. Die size: 890x890 μm^2.

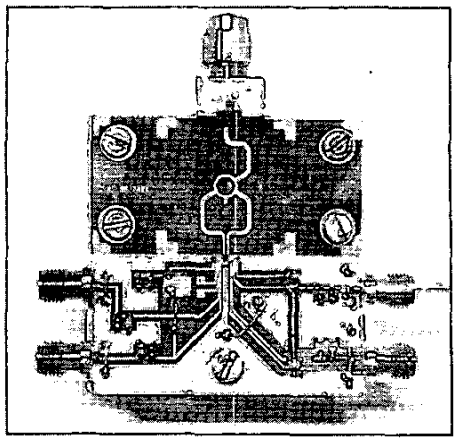


Fig. 8. Demonstrator of VCO and frequency divider. The chip is mounted on a brass block and wire-bonded to external gold-plated microstrip lines on RT/Duroid.

divider of 19.7 GHz is close to the 19.3 Ghz of simulated self-resonance frequency from a simulation of the divider with parasitic capacitances added to the circuit. This indicates a high quality of the parasitic extraction. Fig. 5 shows the measured tuning range and output power of the VCO. Measured single-ended output power at the balun varies between 0.35 and 2.35 dBm without calibrating the losses of bias-T, connectors and cable. The variation of the output power is attributed to double reflections of the output signal cancelling some of the output power. The characteristic sine-shape of the output-power vs. frequency curve together with a slight monotonic decrease of output power with tuning voltage obtained from simulations, supports this assumption. Currently, no measurement data is available for the VCO with on-chip output terminations to counteract this effect, however the output-power is expected to vary less when this measure is taken. Fig. 6 shows the frequency spectrum of the free-running VCO at a tuning voltage of 0 V, as well as the transient output signal of the VCO and the frequency divider. Phase-noise performance as measured with a spectrum-analyzer is approximately -85 dBc/Hz at an offset frequency of 1 MHz. For 10 MHz offset frequency, the phase noise is -105 dBc/Hz, corresponding to a 20 dB/decade slope.

IV. Conclusion

The design and implementation of a single-chip VCO and frequency divider for RADAR applications was presented. Based on an LC-type oscillator with varactor tuning, the design offers a compact and area-efficient solution for a RADAR transmitter. One of the key features is the ease of use together with a standard PLL-circuit for the 1.5 GHz range. The total power consumption from a 3.6 V supply is 12 mA for the VCO, 17 mA for the frequency divider and 51 mA for the output driver, corresponding to a total of 288 mW. Measured phase-noise performance is approximately -85 dBc/Hz at an offset frequency of 1 MHz, the frequency is tuneable from 20.3 GHz to 20.9 GHz.

Acknowledgements

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